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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/616,810	07/10/2003	Mark E. Schuelein	1000-0011	2270

7590 03/16/2005

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EXAMINER	
NGUYEN, MINH T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 03/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/616,810	SCHUELEIN, MARK E.	
	Examiner	Art Unit	
	Minh Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,9-15,22,26-29 and 31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11,12,27-29 and 31* is/are allowed.

6)☒ Claim(s) *1-5,9,10,13-15,22 and 26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's amendment filed on 2/28/05 has been received and entered in the case. Claims 1-5, 9-15, 22, 26-29 and 31 are pending. New ground of rejections necessitated by the amendment is set forth below. This action is FINAL.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5, 9-10, 13-15, 22 and 26 rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,566,927, issued to Park et al. in view of US Patent No. 6,433,601, issued to Ganesan.

As per claim 1, Park discloses a flip-flop (Fig. 12), comprising:

a state retention portion (1130) to store a bit of digital data (the data D), having a first storage node (the node connected to the input of inverter 1132) and a second storage node (the node connected to the output of inverter 1132); and

a clocking portion (the combination of circuits 1210 and 1120) to transfer a new bit of digital data (D) to the state retention portion (1130) in response to a clock signal (CLK), the clocking portion including:

a first stack of transistors (1121 and 1122) coupled to the first storage node (the node connected to the input of inverter 1132) to function as recited, the first stack of transistors including a first transistor (1121) having a gate terminal coupled to receive said clock signal (CLK) and a second transistor (1122) having a gate terminal coupled to receive a delayed, inverted version of said clock signal (by the delayed, inverted circuit 1210).

wherein said clocking portion comprises a clock node (the node to receive the clock signal CLK) to receive said clock signal and an inversion device (1210) coupled between said clock node and said gate of said second transistor (as shown, the output of the inversion device 1210 provides signal to the gate of the second transistor 1122), wherein said inversion device includes a NOR gate (NOR gate 1213) having first and second input terminals and an output terminal, said first input terminal (the input terminal which receives the clock signal CLK through inverters 1211 and 1212) being connected to said clock node, said output terminal being connected to said gate terminal of said second transistor (the output of NOR gate 1213 provides signal to the gate of the second transistor 1122), and said second input (the input terminal of NOR gate 1213 to receive the signal AF) being an enable input of said flip flop.

Park further explicitly discloses the first transistor 1121 and second transistor 1122 are cascoded and functioned as complementary switches (see Fig. 5). As shown in Fig. 12, it is clear that the data signal at the output terminal of transistor 1122 follows the date signal at the input terminal of transistor 1122 when the clock signal CLKB makes a transition from low to high which is a result of the clock signal CLK makes a transition

from high to low (falling edge of the CLK signal). Thus the flip-flop shown in Fig. 12 is a negative-edge triggered flip-flop.

Park does not explicitly disclose the first transistor 1121, which has a gate for receiving the clock signal CLK, is directly connected to the first storage node as called for in the claim. In other words, the recited configuration provides a positive-edge triggered flip-flop.

Ganesan teaches a flip-flop circuit (Fig. 5) which includes a state retention portion 420 and a clocking portion. The clocking portion includes a first transistor T1 having a gate for receiving a clock signal and second transistor T3 having a gate for receiving a delayed version of the clock signal wherein the first transistor T1, which has a gate for receiving the clock signal CLK, is directly connected to the first storage node of the state retention portion 420. He further discloses that having the gate of transistor T1 receives the clock signal and the gate of transistor T3 receives the delayed version of the clock signal, the data signal at the output terminal of transistor T1 follows the date signal at the input terminal of transistor T1 when the clock signal makes a transition from low to high (column 6, lines 50-55, rising edge of the clock signal). Thus the Ganesan's flip-flop is a positive-edge triggered flip-flop.

As known by a person skilled in the art, negative-edge triggered flip-flops are widely used, so as positive-edge triggered flip-flops. Some applications require negative-edge triggered flip-flops and some applications require positive-edge triggered flip-flops.

It would have been obvious to one skilled in the art at the time of the invention was made to provide the clock signal CLK to transistor 1122 and the clock signal CLKB which is a delayed inverted version of the clock signal CLK to transistor 1121 in the

Park's flip-flop as taught by Ganesan. The motivation and/or suggestion would be to change the Park's flip-flop from a negative-edge triggered flip-flop to a positive-edge triggered flip-flop so that the Park's flip-flop can be used in applications which require positive-edge triggered flip-flops.

As per claim 2, as shown in Fig. 12, transistors 1121 and 1122 are IGFETs.

As per claim 3, the recited second stack of transistors which are third and fourth transistors read on transistors 1124 and 1123, respectively. The reason for providing the clock signal CLK to transistor 1124 and the clock signal CLKB to transistor 1123 and the motivation for switching are the same as discussed in claim 1.

As per claim 4, as shown in Fig. 12, transistors 1123 and 1124 are IGFETs.

As per claim 5, Fig, 12 clearly shows the connections of the gate terminals of transistors 1121-1124 as recited.

As per claims 9-10, the circuit 1130 has only one latch having two inverters 1131 and 1132 crossed coupled.

As per claim 13, the recited next state generation portion reads on inverter 1150. Since the D signal is not part of the flip-flop, the D signal is seen as signal from an external source supplied to the flip-flop.

As per claim 14, the recited inversion device reads on inverter 1150.

As per claim 15, the recited input node reads on the node receiving the D signal, the recited first inversion device reads on inverter 1150.

As per claim 22, this claim is merely a method to operate a flip-flop having the structure discussed in claim 3, since the structure discussed in claim 3 teaches the circuit, the method to operate is obvious.

As per claim 26, this claim is rejected for the same reason noted in claim 10.

Response to Arguments

3. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

4. Claims 11-12, 27-29 and 31 are allowed.

Claims 11-12 are allowed because the prior art of record fails to disclose or suggest the inclusion of first and second pull-up circuits wherein the first pull-up circuit having first and second transistors connected in parallel to provide separate pull-up paths for the first inverter as recited in claim 11.

Claims 27-29 and 31 are allowed for the same reason noted in claim 11.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is 571-272-1748. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

3/11/05

Minh Nguyen
Primary Examiner
Art Unit 2816